REMARKS

I. Introduction

At the time of the Office Action dated June 5, 2006, claims 1-29 were pending in this application. In this Amendment, claims 1, 8, 14, 16, 18-20, 22-24 and 26-29 have been amended, and claims 2 and 15 have been canceled. Care has been exercised to avoid the introduction of new matter. Specifically, claims 1 and 14 have been amended to include all the limitations recited in claims 2 and 15, respectively. Claim 27 has also been amended in a manner as the amendment made to claims 1 and 14. Claims 8, 16, 18-20, 22-24 and 26-29 have been amended to correct minor errors.

II. The Rejection of the Claims under 35 U.S.C. §102(b)

Claims 1, 3, 5, 7, 9, 11, 13, 14, 16, 18, 20, 22, 24 and 26-29 have been rejected under 35 U.S.C. §102(b) as being anticipated by Yonezawa et al. It is noted that since independent claims 1 and 14, as well as claim 27, have been amended to include the limitations recited in claims 2 and 15, respectively, those independent claims and their dependent claims are discussed later. Here, Applicant will discuss patentability of claims 5, 7, 9, 11, 18, 20, 22, 24, 28 and 29.

It is well established precedent that the factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *See Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

Applicant submits that Yonezawa et al. does not disclose a system LSI design support apparatus including all the limitations recited in independent claim 5. Specifically, Yonezawa et al. does not disclose, at a minimum, "an analyzer, which counts the number of loop control statements," as recited in claim 5. The present invention makes it possible to adequately assign features to a system LSI comprising processing units having a plurality of different architectures.

Yonezawa et al. discloses calculating the number of cycles of loop control statements (column 10, lines 22-26). However, calculating the number of cycles of loop control statements is different from calculating the number of loop control statements, as claimed. Yonezawa teaches calculating how many times the same operation is repeated by the loop control statement. In contrast, claim 5 recites counting the number of loop control statements.

Accordingly, Yonezawa et al. does not identically disclose a system LSI design support apparatus including all the limitations recited in independent claim 5. The above discussion is applicable to independent claims 9, 18, 22, 28 and 29. Dependent claims 7, 11, 20 and 24 are also patentably distinguishable over Yonezawa et al. at least because these claims include all the limitations recited in independent claims 5, 9, 18 and 22, respectively. Applicant, therefore, respectfully solicits withdrawal of the rejection of claims 5, 7, 9, 11, 18, 20, 22, 24, 28 and 29 under 35 U.S.C. §102(b) and favorable consideration thereof.

III. The Rejection of Claims under 35 U.S.C. §103(a)

Claims 2, 4, 6, 8, 10, 12, 15, 17, 19, 21, 23 and 25 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yonezawa et al. in view of Gutberlet et al. Since the limitations of claims 2 and 15 have been incorporated into independent claims 1 and 14, as well

as independent claim 27, in this Amendment, Applicant will discuss patentability of independent claims 1, 14 and 27 below.

In the statement of the rejection, the Examiner admitted that Yonezawa et al. does not disclose the use of nestings of conditional branch statements. However, the Examiner asserted that Gutberlet et al. teaches the missing feature of Yonezawa et al., and concluded that it would have been obvious to modify Yonezawa's device in view of the teachings of Gutberlet et al. to arrive at the claimed invention.

Applicant submits that the applied combination of Yonezawa et al. and Gutberlet et al. does not teach a system LSI design support apparatus including all the limitations recited in independent claim 1, as amended. Specifically, the applied combination does not teach, at a minimum, counting the number of nestings of the conditional branch statements, as recited in claim 1.

Yonezawa et al. discloses dividing a description part into S/W and H/W blocks based on the number of conditional branchs (column 10, lines 6-16). As admitted by the Examiner, Yonezawa is silent on counting the number of nestings of the conditional branch statements, as claimed.

Gutberlet et al. teaches hardware description with nestings. However, Gutberlet et al. does not teach nestings in conditional branch statements, but nestings in loop control statements (see paragraph [0005]). Furthermore, Gutberlet et al. does not teach counting the number of nestings. In contrast, claim 1 recites counting the number of nestings of the conditional branch statements.

Accordingly, the applied combination of Yonezawa et al. and Gutberlet et al. does not teach a system LSI design support apparatus including all the limitations recited in independent

claim 1, as amended. The above discussion is applicable to independent claims 14 and 27 reciting the number of nestings of the conditional branch statements.

Dependent claims 3, 4, 6, 8, 10, 12, 13, 16, 17, 19, 21, 23, 25 and 26 are also patentably distinguishable over Yonezawa et al. and Gutberlet et al. at least because these claim include all the limitations recited in independent claims 1, 5, 9, 14, 18 and 22.

Applicant, therefore, respectfully solicits withdrawal of the rejection of claims 1, 3, 4, 6, 8, 10, 12-14, 16, 17, 19, 21, 23, 25 and 27, and favorable consideration thereof.

IV. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:TT
Facsimile: 202.756.8087
Date: September 5, 2006
WDC99 1278905-1.061282.0064